Technical Information Manual

Revision n. 3
5 September 2002

MOD. V820 series
MOD. V830 series
32 CHANNEL
LATCHING
SCALERS

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1. General description

1.1. Overview

The models **V820** and **V830** are 1-unit wide VME 6U Latching Scaler and Multievent Latching Scaler modules, housing 32 independent counting channels.
Each channel has 32 bit counting depth and accepts either ECL or LVDS inputs, depending on the purchased version, a TTL version is available on request; the maximum input frequency is 250 Mhz.

The counters' values can be read "on the fly" from VME without interfering on data acquisition process.
The model **V830** is equipped with a 32 kwords multievent buffer (MEB) memory which may be used to store and readout accumulated data during subsequent counting.
The TRIGGER signal can be provided by an external NIM/ECL signal or by a VME request. It's also possible to generate a periodical trigger signal by means of an internal programmable timer.
The modules feature **VETO** and **CLEAR** ECL inputs and a **TEST** NIM input (in common for all channels).

The model **V820** works in A24/A32 mode and data transfer occurs in D32 mode. The unit also supports the Multicast commands. The model **V830** works in A24/A32 mode and data transfer occurs in D32, BLT32 or MBLT64 mode. The unit also supports the Chained Block Transfer (CBLT32/CBLT64) and the Multicast commands.

Several modules' versions are available, please refer to Table 1.1 for details.

All the models have a special circuitry that allows the board to be removed from and inserted in a powered crate without switching the crate off (**Live Insertion**).

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Table 1.1: Versions available for V820 / V830 modules

Version[1]	Number of channels	PAUX connectors[2]	-5 V DC/DC converter	MEB	Live Insertion	Input type
V820 AA[3]	32	Yes	No	No	Yes	ECL
V820 AC[3]	32	No	Yes	No	Yes	ECL
V820 LA[3]	32	Yes	No	No	Yes	LVDS
V820 LC[3]	32	No	Yes	No	Yes	LVDS
V830 AA[3]	32	Yes	No	Yes	Yes	ECL
V830 AC	32	no	Yes	Yes	Yes	ECL
V830 LA[3]	32	Yes	No	Yes	Yes	LVDS
V830 LC	32	no	Yes	Yes	Yes	LVDS

Fig. 1.1: Model type label (example V830 AC)

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[1] A label on the printed board soldering side indicates the module's version (see Fig 1.1).

[2] The versions with the PAUX connector require the V430 backplane.

[3] Model available exclusively on request.

1.2. Block diagram
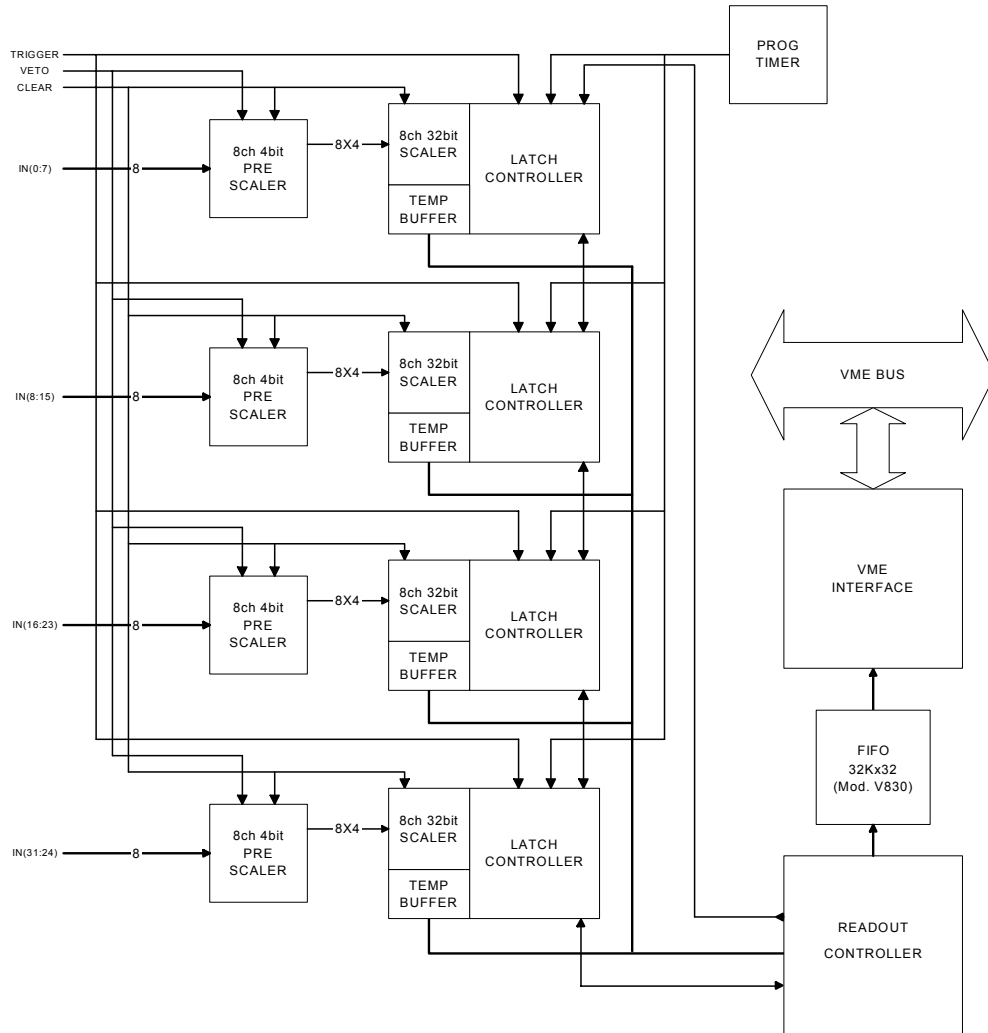
Fig. 1.2: Model V820/V830 Block Diagram

2. Technical specifications

2.1. Packaging

The Models V820 and V830 are housed in a 6U-high, 1U-wide VME unit. The versions equipped with the PAUX connector (**V820 AA / LA** and **V830 AA / LA**) require the VME V430 backplane.

2.2. Power requirements

All the models available for the V820/V830 modules need +5V and –5V power supplies. The versions without the PAUX connector (**V820 / V830 AC / LC**) have a DC-DC converter for the –5V power line.

Table 2.1: Power requirements

Power supply	V820 AA	V830 AA	V820 AC	V830 AC	V820 LA	V830 LA	V820 LC	V830 LC
+5 V	1.1 A	1.1 A	2.5 A	2.5 A	TBD	TBD	1 A	1 A
-5 V	1 A	1 A	-	-	TBD	TBD	-	-

2.3. Front Panel
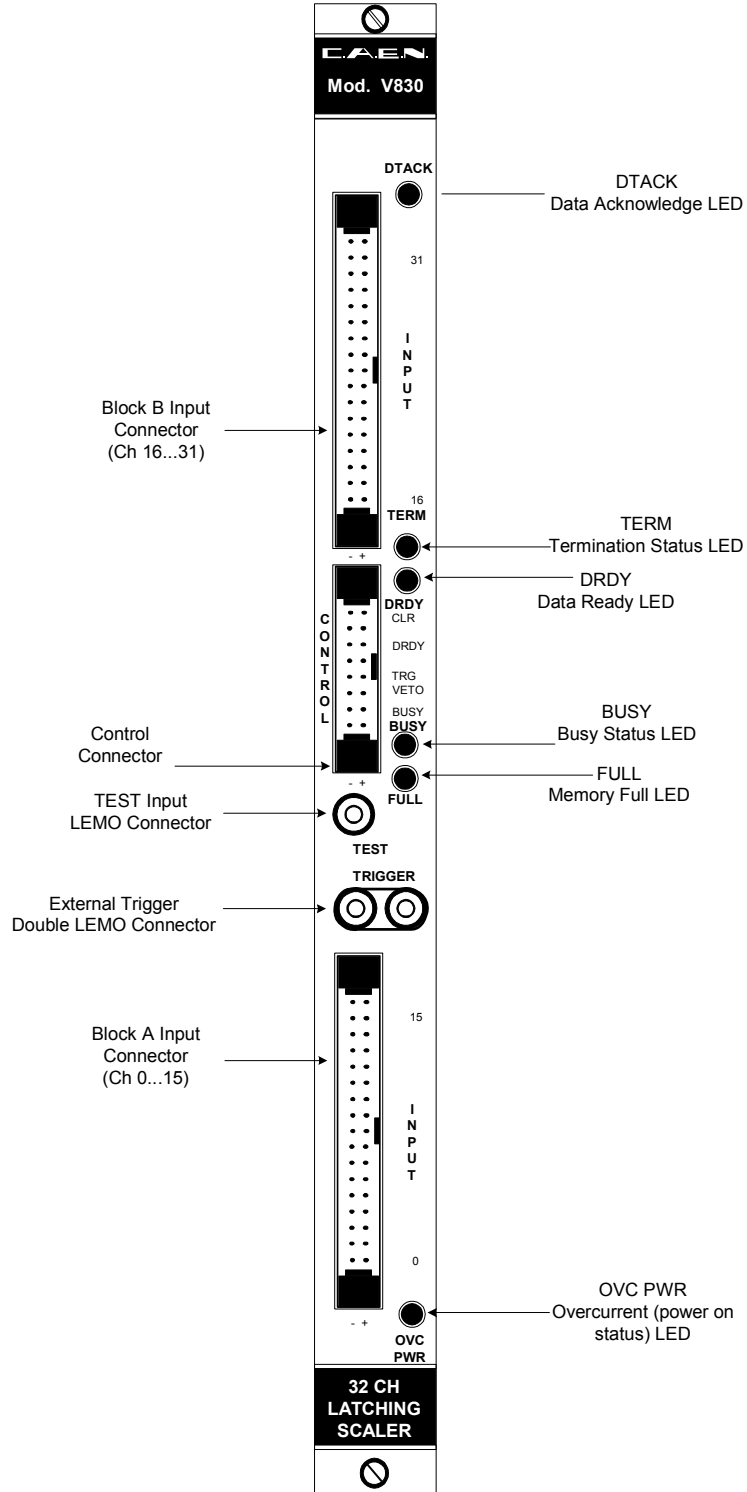
Fig. 2.1: Model V820/V830 front panel

2.4. External connectors

The location of the connectors is shown in Fig. 2.1. Their function and electro-mechanical specifications are listed in the following subsections.

2.4.1. INPUT connectors

Mechanical specifications:
two 17+17-pin, 3M 7634-5002 Header-type connectors.
Electrical specifications:
V820 / V830 AA / AC: ECL input signals, rising edge, 110 Ω impedance. The highest pair of pins of each connector is not connected.
V820 / V830 LA / LC: LVDS input signals, rising edge, 110 Ω impedance. The highest pair of pins of each connector is not connected.

BLOCK A INPUT: input signals from channel 0 through channel 15.

BLOCK B INPUT: input signals from channel 16 through channel 31.

N.B.: in the V820 / V830 LA / LC (LVDS inputs), if no input signal is present (i.e. the channels are disconnected), the channels' logic status is "1".

2.4.2. CONTROL connector

Mechanical specifications:
one 8+8-pin, 3M 7616-5002 Header-type connectors.

Pin assignment is shown in Fig. 2.2. The lowest pair of pins is not connected: they can be optionally connected to VEE (-5 V) or to DIGITAL GND by means of a soldering pad on the Printed Circuit Board (see § 2.6.2). All the control lines described below can be 110 Ω terminated on-board via internal DIP-switches, see § 2.6.1 for further details.

CLR: *Electrical specifications:* differential. ECL input signal, active-high; high impedance; min width: 10 ns.
Function: CLEAR signal, clears all the counters. If the bit 6 (CLRMEB) of the Control Register is set the MEB memory is cleared too (for **V830** module only).

DRDY: *Electrical specifications:* differential. ECL input/output signal, active-high; high impedance.
Function: indicates the presence of data in the MEB of the **V830** board; DATA READY status is also flagged by the bit 0 of the Status Register; when several boards are daisy-chained via the CONTROL connector, the wired OR and NAND of DATA READY signals can be read respectively on the DRDY+ and DRDY- lines of the CONTROL bus and the status of the DRDY+ bi-directional line is flagged by the bit 3 (G_DRDY) of the Status Register (see § 3.11).

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TRG: *Electrical specifications:* differential. ECL input signal, trailing edge; high impedance; min. width: 10 ns.
Function: TRIGGER signal for "on the fly" scalers data latching. Mod. **V830**: an event is also written into the MEB when TRG occurs.

VETO: *Electrical specifications:* differential. ECL input signal, active-high; high impedance.
Function: inhibits counting on all the channels.

BUSY: *Electrical specifications:* differential. ECL input/output signal, active-high; high impedance.
Function: Mod. **V830**: the board is writing data in the MEB memory; duration: 1 µs (independently from the number of enabled channels). It also actives when the MEB memory is full. When BUSY status is met TRIGGER signals are neglected.
Mod. **V820**: the board is writing data in the local buffer and cannot accept a trigger signal; duration: 150 ns.
When several boards are daisy-chained, the wired OR and NAND of BUSY signals can be read respectively on the BUSY+ and BUSY- lines of the CONTROL bus and the status of the BUSY+ bi-directional line is flagged by the bit 4 of the Status Register (see § 3.11).

/ CLR ← (16)	(15) → CLR
not connected ← (14)	(13) → not connected
/ DRDY ← (12)	(11) → DRDY
not connected ← (10)	(9) → not connected
/ TRG ← (8)	(7) → TRG
/ VETO ← (6)	(5) → VETO
/ BUSY ← (4)	(3) → BUSY
not connected (S5) ← (2)	(1) → not connected (S6)
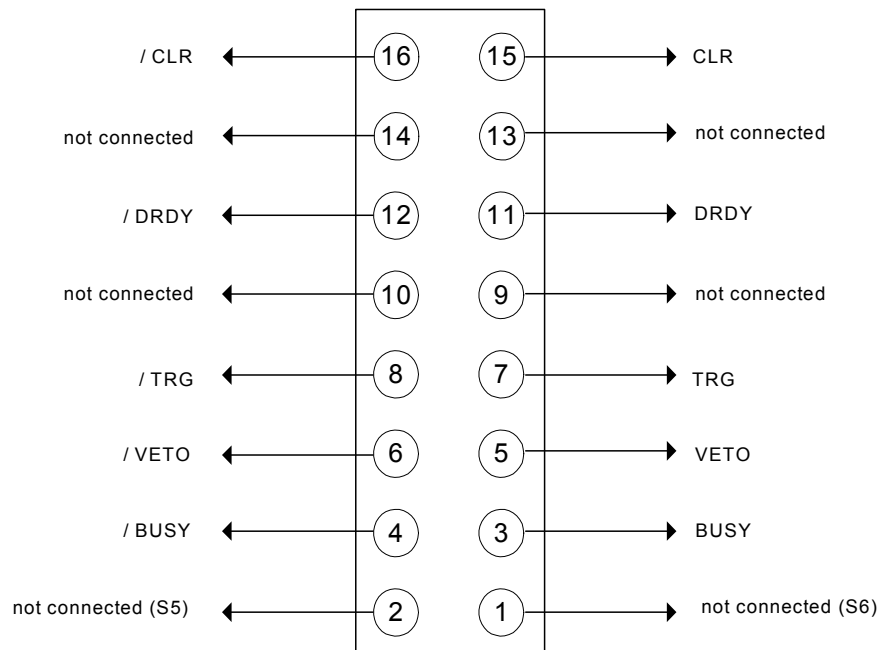
Fig. 2.2: CONTROL connector pin assignment

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2.4.3. TRIGGER connector

TRIGGER: *Mechanical specifications:* Two bridged LEMO connectors.
Electrical specifications: NIM std. input signals, trailing edge; high impedance; min. width: 10 ns. (If this input is used, a 50 Ω termination is required; in daisy-chain configuration, the termination must be inserted on the last board of the chain)
Function: TRIGGER signal for "on the fly" scalers data latching. Mod. **V830**: an event is also written into the MEB when TRG occurs.
N.B.: this input is ORed with the TRG signal on the CONTROL connector.

2.4.4. TEST connector

TEST: *Mechanical specifications:* LEMO type connector.
Electrical specifications: NIM std. input signals, active high; high impedance;
Function: TEST signal common for all counters.

2.4.5. Mod. V820/V830 data loading timing diagram

The following diagram shows the Mod. V820/V830 data loading operation sequence:
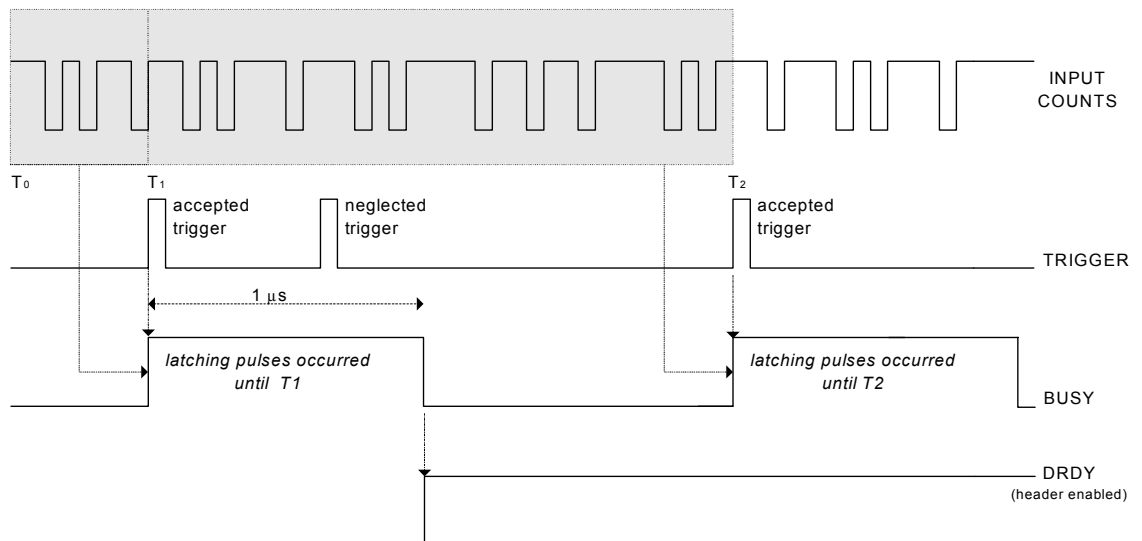
Fig. 2.3: Mod. V820/V830 data loading diagram

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2.5. Other front panel components

2.5.1. Displays

The front panel (refer to Fig. 2.1) hosts the following LEDs:

DTACK:
Colour: green.
Function: DATA ACKNOWLEDGE command; it lights up each time a VME access is performed. It also lights up for a while at power ON to indicate that the board is configuring.

TERM:
Colour: orange/green/red.
Function: it lights up green when all the lines of the control bus are terminated, red when no line of the control bus is terminated. If only some lines are terminated, it is off.

DRDY:
Colour: green.
Function: it lights up when data are stored in memory; it also lights up for a while at power ON to indicate that the board is configuring.

BUSY:
Colour: red.
Function: it lights up when the module is busy (see § 2.4.2); it also lights up for a while at power ON to indicate that the board is configuring.

FULL:
Colour: red.
Function: it lights up each time the Multi-Event Buffer is full (Mod. V830 only); it also lights up for a while at power ON to indicate that the board is configuring.

OVC/PWR:
Colour: green/orange.
Function: it lights up green when the board is inserted into the crate and the crate is powered up; when it is orange, it indicates that there is an over-current status.

2.6. Internal hardware components

In the following some hardware setting components, located on the boards, are listed. Refer to Fig. 2.4 and Fig. 2.5 for their exact location on the PCB and their settings.

2.6.1. Switches

ROTARY SWITCHES:
Type: 4 rotary switches.
Function: they allow to select the VME base address of the module. Please refer to Fig. 2.4 for their settings.

TERM ON:
Type: 10 DIP switches, a couple (positive and negative) for each control signal.
Function: they allow the insertion of the Bus termination on the relevant line. The 110 Ω-termination must be inserted on

the lines of the last board of the chain. In order to insert the termination on a given line, both the positive and the negative DIP switches must be set (see Fig. 2.4).

Right position (dot visible): the termination is inserted on the relevant line;

Left position (dot not visible): the termination is not inserted.

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**Rotary switches for
VME address
selection**

Base address bit <19~16>

Base address bit <23~20>

Base address bit <27~24>

Base address bit <31~28>

DIP switches for
BUS termination insertion

TERM   ON

CLR

/ CLR

DRDY

/ DRDY

TRG

/ TRG

VETO

/ VETO

BUSY

/ BUSY

Right position (dot visible)
termination ON

Right position (dot not visible)
termination OFF

Fig. 2.4: Components Location (components side)

2.6.2. Soldering pads

S5 (VEE): *Function:* it allows to connect the second pin of the CONTROL connector to the VEE power supply (-5 V).

> ***No Soldering*** (default): the pin 2 of the CONTROL connector is not connected.
> ***Soldering***: the pin 2 of the CONTROL connector is connected to VEE power supply (-5 V).

S6 (GND): *Function:* it allows to connect the first pin of the CONTROL connector to the DIGITAL GROUND.

> ***No Soldering*** (default): the pin 1 of the CONTROL connector is not connected.
> ***Soldering***: the pin 1 of the CONTROL connector is connected to the digital ground.

See Fig. 2.5 for the exact location of these pads on the PCB and their settings
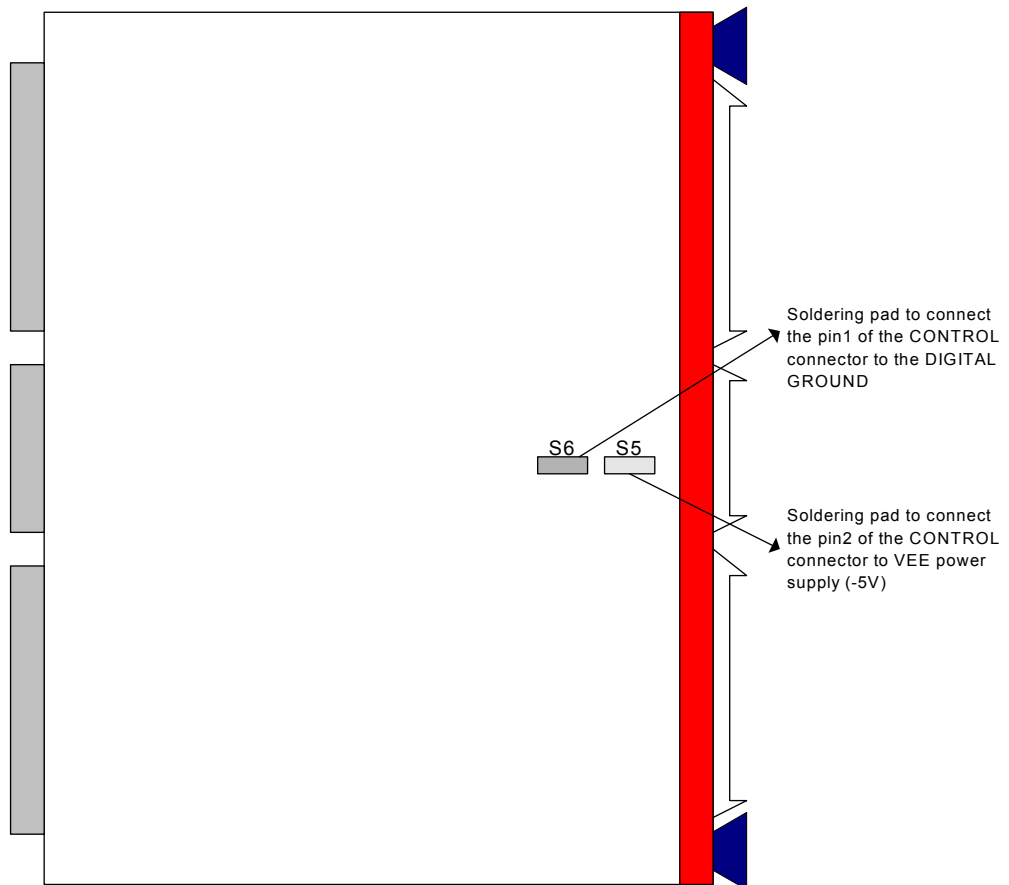
Fig. 2.5: Components location (soldering side)

2.7. Technical specifications table

Table 2.2: Model V820/V830 technical specifications

Packaging	6U-high, 1U-wide VME unit (version AA/LA require the V430 crate)
Power requirements	See Table 2.1
Inputs	32 ECL/LVDS (TTL on request), depending on version, 110 Ω
Maximum Counting Rate	250 Mhz
Channel depth	32 significant bits for "on the fly" readout
Dwell Time	Internal programmable 32-bit timer in 400 ns steps
Trigger	External, internal with programmable timer, internal via VME access
Event Memory	Mod. **V830**: 32 kwords (128 kbytes) multievent buffer (MEB)
TRIGGER input	Two bridged LEMO connector, NIM signal, min. width 30 ns, high impedance
TEST input	One LEMO connector, NIM signal, high impedance, common to all channels
Control inputs	active-high, differential ECL input signals: **CLR:** clear of all the scalers, min. width 10 ns **TRG:** signal for "on the fly" scalers data latching, min. width 10 ns **VETO:** inhibits all the counters
Control outputs	differential ECL output signals: **DRDY:** indicates the presence of data in the MEB (for **V830**) **BUSY:** indicates that the module is busy and refuses triggers
Displays	**DTACK:** green LED; lights up at each VME access. **TERM:** orange/green/red LED; alight according to line termination status **DRDY:** green LED; alight as there is one event in the MEB (for **V830**) **BUSY:** red LED; it signals that the module is busy and ignores incoming triggers **FULL:** red LED; alight when the MEB is full **OVC/PWR:** green/orange LED; green at board insertion; if orange, it indicates that there is an over-current status.
VME interface	**Addressing**: A24, A32 **Data Transfer**: D16, D32, BLT32, BLT64, CBLT32, CBLT64 **Geographical addressing** **Multicast commands**

3. VME Interface

The following sections will describe in detail the board's VME-accessible registers' content.

3.1. Registers address map

Table 3.1: Register address map

REGISTER	ADDRESS	ADDRESS MODE	DATA MODE	TYPE
MEB (Mod. V830)	0x0000÷	A24/A32	D32	Read only
Counter 0	0x1000	A24/A32	D32	Read only
Counter 1	0x1004	A24/A32	D32	Read only
Counter 2	0x1008	A24/A32	D32	Read only
Counter 3	0x100C	A24/A32	D32	Read only
Counter 4	0x1010	A24/A32	D32	Read only
Counter 5	0x1014	A24/A32	D32	Read only
Counter 6	0x1018	A24/A32	D32	Read only
Counter 7	0x101C	A24/A32	D32	Read only
Counter 8	0x1020	A24/A32	D32	Read only
Counter 9	0x1024	A24/A32	D32	Read only
Counter 10	0x1028	A24/A32	D32	Read only
Counter 11	0x102C	A24/A32	D32	Read only
Counter 12	0x1030	A24/A32	D32	Read only
Counter 13	0x1034	A24/A32	D32	Read only
Counter 14	0x1038	A24/A32	D32	Read only
Counter 15	0x103C	A24/A32	D32	Read only
Counter 16	0x1040	A24/A32	D32	Read only
Counter 17	0x1044	A24/A32	D32	Read only
Counter 18	0x1048	A24/A32	D32	Read only
Counter 19	0x104C	A24/A32	D32	Read only
Counter 20	0x1050	A24/A32	D32	Read only
Counter 21	0x1054	A24/A32	D32	Read only
Counter 22	0x1058	A24/A32	D32	Read only
Counter 23	0x105C	A24/A32	D32	Read only
Counter 25	0x1064	A24/A32	D32	Read only
Counter 26	0x1068	A24/A32	D32	Read only
Counter 27	0x106C	A24/A32	D32	Read only
Counter 28	0x1070	A24/A32	D32	Read only
Counter 29	0x1074	A24/A32	D32	Read only
Counter 30	0x1078	A24/A32	D32	Read only
Counter 31	0x107C	A24/A32	D32	Read only
Testreg	0x1080	A24/A32	D32	Read/Write
Testlcnth	0x1094	A24/A32	D16	Read/Write

REGISTER	ADDRESS	ADDRESS MODE	DATA MODE	TYPE
Testhcntl	0x10A0	A24/A32	D16	Read/Write
Testhcnth	0x10A4	A24/A32	D16	Read/Write
Channel Enable	0x1100	A24/A32	D32	Read/Write
Dwell Time	0x1104	A24/A32	D32	Read/Write
Control Register	0x1108	A24/A32	D16	Read/Write
Bit Set Register	0x110A	A24/A32	D16	Write only
Bit Clear Register	0x110A	A24/A32	D16	Write only
Status Register	0x110E	A24/A32	D16	Read/Write
GEO Register	0x1110	A24/A32	D16	Read/Write
Interrupt Level	0x1112	A24/A32	D16	Read/Write
Interrupt Vector	0x1114	A24/A32	D16	Read/Write
ADER_32	0x1116	A24/A32	D16	Read/Write
ADER_24	0x1118	A24/A32	D16	Read/Write
Enable ADER	0x111A	A24/A32	D16	Read/Write
MCST Base Address	0x111C	A24/A32	D16	Read/Write
MCST Control	0x111E	A24/A32	D16	Read/Write
Module Reset	0x1120	A24/A32	D16	Read/Write
Software Clear	0x1122	A24/A32	D16	Write only
Software Trigger	0x1124	A24/A32	D16	Write only
Trigger Counter	0x1128	A24/A32	D16	Write only
Almost Full Level	0x112C	A24/A32	D16	Read/Write
BLT event number	0x1130	A24/A32	D16	Read/Write
MEB event number	0x1134	A24/A32	D16	Read only
Dummy32	0x1200	A24/A32	D32	Read/Write
Dummy16	0x1204	A24/A32	D16	Read/Write
Configuration ROM	0x4000	A24/A32	D16	Read only
Firmware	0x1132	A24/A32	D16	Read only

3.2. Memory Event Buffer (MEB) Register (V830 only)

(Base Address + 0x0000 ÷ + 0x0FFC, D32, BLT32/64, CBLT32/64, read only)

This register allows to access the Multiple Event Buffer to readout (in D32, BLT32/64, or CBLT32/64 mode) the data values.
The MEB contains the output data organised in 32-bit words.
The data in the buffer are organised in events. Each event consists of the **header** (32-bit word) and one or more **data words** (up to 32).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GEO					1			N. WORDS						TS		TRIGGER NUMBER															

TS = 00: external trigger
TS = 01: trigger via timer
TS = 10: trigger via VME

Fig. 3.1: MEB: the Header
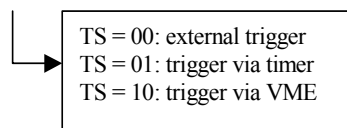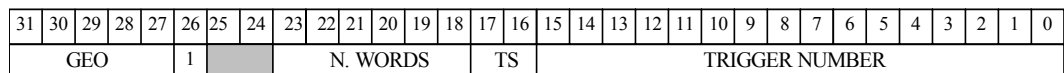
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
													CHANNEL COUNTER																		
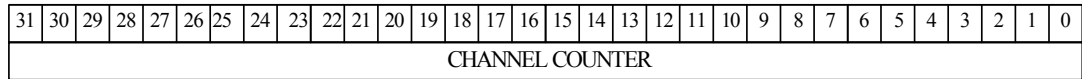
Fig. 3.2: MEB: the data word format in 32 bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHANNEL					0									CHANNEL COUNTER																
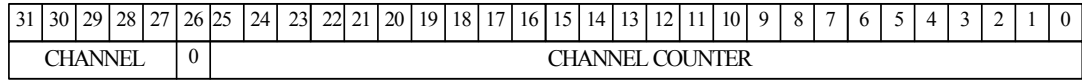
Fig. 3.3: MEB: the data word format in 26 bit

Header content:

The bits[31…27] contains the GEO address.

The bit 26 is the Header identifier.

The bits 25 and 24 are meaningless.

The bits[23..18] identify the number of enabled channels;

The bits 17 and 16 identify the trigger source.

The bits[15…0] contain the progressive trigger number.

Datum content:

- **32-bit format (Fig. 1.2)**

  The entire counter value is written in the MEB for each channel. No additional information (channel number, etc.) can be saved. Not possible to flag differently the header and the datum.

- **26-bit format (Fig. 1.3)**

  Only 26 bits of the counter value is written in the MEB for each channel. Additional information (channel number, etc.) can be saved. The header and the datum can be distinguished via bit 26.

N.B.: the channel depth is always 32 bits. The datum 26-bit format refers to the channel counter writing in the MEB. "Fillers" (see § 4.6.2) are managed as valid data.

3.3. COUNTER0 – COUNTER31

(Base Address + 0x1000 ÷ 0x107C, D32, read)

These registers contain the 32 bit counters value.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
													CHANNEL COUNTER																	

Fig. 3.4: Data word format for each counter

These registers support D32 accesses only.

3.4. Test Register (V830 only)

(Base Address + 0x1080, D32, read/write)

When the module works in Test Mode (bit 3 of the Control Register set to 1, see § 3.8) and TRIGGER is enabled in *random mode* (see § 3.8), an event, composed of 32 words sharing the same content in the 5…31 bits (set by the user)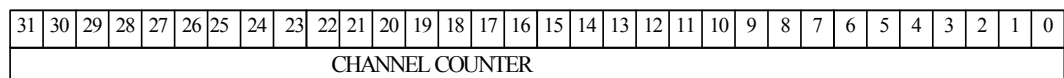 and having the number of channel, ranging from 0 to 31, in the 0…4 bits of this register (see Fig. 3.5) is written into the MEB after a TRIGGER occurs.
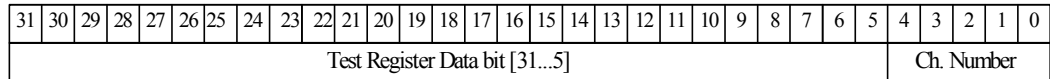
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Test Register Data bit [31...5]																											Ch. Number				

Fig. 3.5: Test register

This register supports D32 accesses. MCST addressing is also allowed.

3.5. Test Counters Registers

(Base Address + 0x1090 ÷ 0x10A4, D16, read/write)

When the module works in Test Mode (bit 3 of the Control Register set to 1, see § 3.8), these registers allow to perform a test of the internal connections: writing the high and low part of a 32-bit test word respectively in the **TESTLOW_CNTLOW** and **TESTLOW_CNTHIGH** registers, it's then possible to read the same 32-bit test word at counters address of the channels 0 through 15. On the other hand, writing the high and low part of a 32-bit test word respectively in the **TESTHIGH_CNTLOW** and **TESTHIGH_CNTHIGH** registers, it's possible to read the same 32-bit test word at counters address of the channels 16 through 31.
This register supports D16 accesses only.
N.B.: Please note that these register are for factory use only.

3.6. Channel ENABLE Register (V830 only)

(Base Address + 0x1100, D32, read/write)

This register allows to enable/disable each channel by writing 1 or 0 in the corresponding register bit.

Bit 0 = Channel 0
Bit 1 = Channel 1   **1 = Channel enabled**
…   **0 = Channel disabled**
Bit 31 = Channel 31

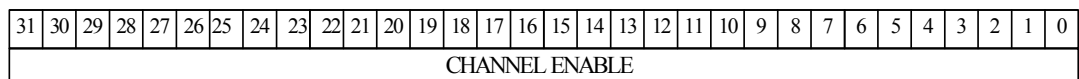| 31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHANNEL ENABLE																															

Fig. 3.6: Channel Enable Register

If a channel is disabled, the counter's value is not transferred from the local buffer into the MEB (although the input pulses' counting proceeds), see Fig. 1.2.
This register supports D32 accesses; the MCST addressing is also allowed.

3.7. Dwell Time Register

(Base Address + 0x1104, D32, read/write)

When the module works with PERIODICAL TRIGGER enabled, (bit 0 and 1 of the Control Register set respectively to 0 and 1, see § 3.8) this register contains the value (N_t) that determines the Dwell Time (T_t), that is the trigger generation period of the internal programmable timer.

Dwell Time = T_t = N_t · 400ns   (being the internal timer stepping = 400 ns)

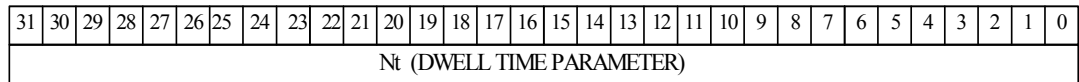| 31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															Nt (DWELL TIME PARAMETER)																

Fig. 3.7: Dwell Time Register

The timer must be programmed with a period larger than the module BUSY time (see § 4.2.3).

This Register must be accessed in D32 mode. MCST access is also allowed.

3.8. Control Register

(Base Address + 0x1108, D16, read/write)

This register allows to set the operation mode of the module.

Fig. 3.8: Control Register

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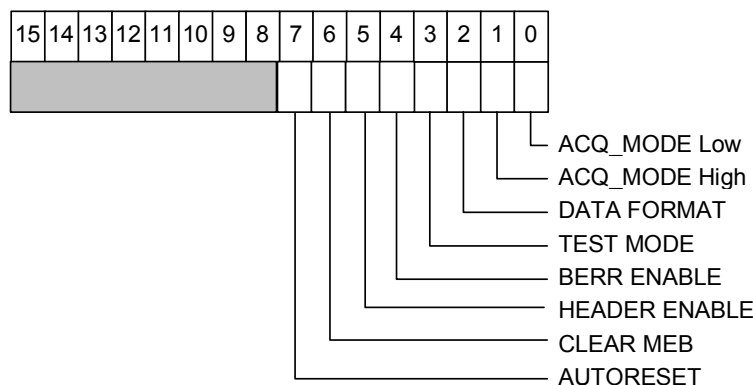ACQ MODE: Selects the ACQUISITION mode.
                           = 00   Trigger disabled (default);
                           = 01   Trigger random (external or from VME);
                           = 10   Periodical Trigger.

DATA FORMAT: Selects the data format (**V830** only, see § 3.2).
                           = 0   32 bit (default);
                           = 1   26 bit.

TEST MODE: Allows to select the acquisition TEST mode (**V830** only).
                           = 0   Test mode OFF (default); normal operation mode
                           = 1   Test mode ON (see § 3.4 and § 3.5)

BERR ENABLE: Bus Error enable bit
                           = 0   BERR disabled (default); the module sends a DTACK signal until the CPU inquires the module;
                           = 1   BERR enabled; the module generates a Bus error to finish a block transfer or to warn that the MEB is empty, when accessed.

HEADER ENABLE: Selects the Header writing in the event (**V830** only).
                           = 0   Header writing disabled(default);
                           = 1   Header writing enabled.

CLEAR MEB: Determines the MEB cleaning after a CLEAR front panel signal (**V830** only).
                           = 0   MEB not cleared after a CLEAR signal (default);
                           = 1   MEB cleared after a CLEAR signal.

AUTO RESET: Allows the automatic counters reset after a trigger.
                           = 0   automatic reset disabled (default);
                           = 1   automatic reset enabled.

(Bits 8 to 15 are meaningless)

This Register must be accessed in D16 mode. MCST access is also allowed.
A read access returns the status of the register. A write access sets the relevant bit to the desired value. After the power ON or after a VME System Reset the Control Register has the following default setting:

                      ACQ MODE = 00 (Trigger disabled)
                      DATA FORMAT = 0 (32 bit)
                      TEST MODE = 0 (test mode OFF)
                      BERR ENABLE = 0 (BERR disabled)
                      HEADER ENABLE = 0 (Header disabled)
                      CLEAR MEB = 0 (MEB not cleared by a CLEAR signal)
                      AUTO RESTART = 0 (no automatic reset after a trigger)

N.B.: a write access to this register causes the Counters Registers, the MEB, the Trigger Counter and the MEB Event Number Register to be cleared.

3.9. Control Bit Set Register

(Base Address + 0x110A, MCST, D16, write only)

This is actually a different way to access the Control Register (see § 3.8). A write access with the bits to 1 sets the relevant bits to 1 in the register. A write access with the bits set to 0 **does NOT clear** the register content: in order to clear the register content, the Bit Clear Register (see § 3.10) must be used (i.e. writing 0x10 to this register sets **only** the BERR ENABLE bit to 1 and doesn't affect the others). This Register must be accessed in D16 mode. MCST access is also allowed.

Fig. 3.9: Control Bit Set Register

N.B.: a write access to this register causes the Counters Registers, the MEB, the Trigger Counter and the MEB Event Number Register to be cleared.

3.10. Control Bit Clear Register

(Base Address + 0x110C, MCST, D16, write only)

This is actually a different way to access the Control Register (see § 3.8). A write access with a bit set to 1 resets that bit. A write access with the bits set to 0 **does NOT clear** the register content, (e.g. writing 0x10 to this register resets **only** the BERR ENABLE bit and doesn't affect the others). This Register must be accessed in D16 mode. MCST access is also allowed.
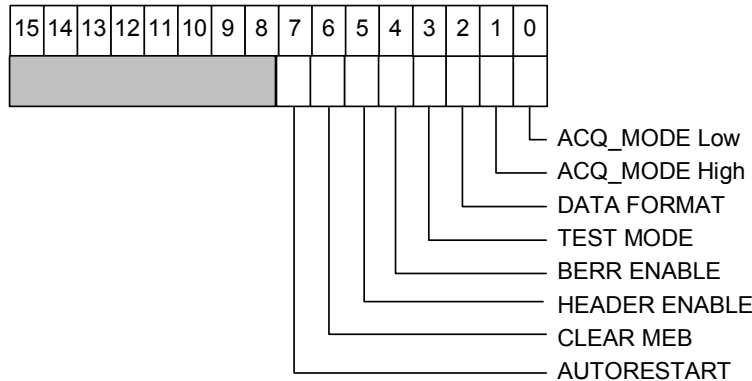**N.B.: a write access to this register causes the Counters Registers, the MEB, the Trigger Counter and the MEB Event Number Register to be cleared.**

3.11. Status Register

(Base Address + 0x110E, D16, read only)

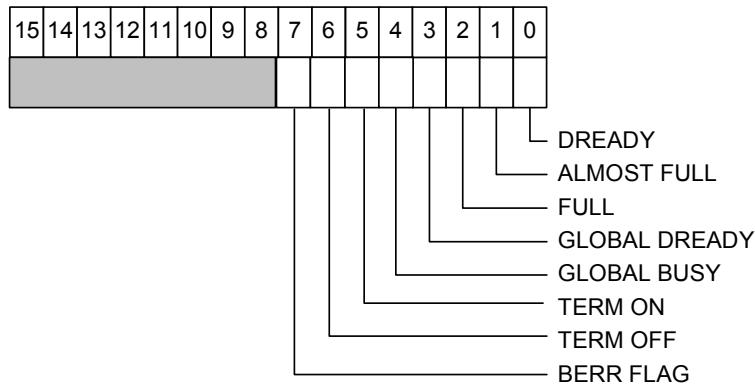This register contains information on the status of the module

Fig. 3.10: Status Register

DREADY (**V830**):   Data Ready bit. _Header enabled:_ this bit indicates that there are events (at least one) in the MEB. _Header disabled_: it indicates that there are data-words (at least one) in the MEB. If the Header is enabled, this register is set when the last word of the last event (datum) is completely written in the MEB. A reset occurs when the last word of the last event has been read. (1 event = header + 32 data-words)
= 0   No events/data (depending on Header) in the MEB;
= 1   Events/data (depending on Header) present in the MEB.

ALMOST FULL (**V830**):   Indicates that the MEB contains at least a number of words equal to the number set in the Almost Full Level register (see § 3.24). If the Almost Full Level of words is reached of the MEB, an Interrupt Request (IRQ) is generated (if enabled), see § 4.4
= 0   There are less words than the Almost Full Level number of words in the MEB;
= 1   There are at least Almost Full Level words in the MEB.

FULL (**V830**):   Indicates that the MEB is full. The MEB is flagged as FULL when it contains 32kwords (MEB size) minus 33words.
= 0   The MEB is not FULL;
= 1   The MEB is FULL.

GLOBAL DREADY (**V830**): When several boards are daisy-chained via the CONTROL connector, it indicates that at least one module in the chain has data in the MEB (wired OR of the READY+ signal of each module in the chain).
= 0   No module has Data Ready:
= 1   At least one module has Data Ready.

GLOBAL BUSY: When several boards are daisy-chained, it indicates that at least one module in the chain is BUSY (wired OR of the BUSY+ signal of each module in the chain). When only one module is used, it indicates that the module is BUSY.
= 0   No module is BUSY:
= 1   At least one module is BUSY.

TERM ON: Termination ON bit. It refers to the termination of the CONTROL bus lines. The insertion or removal of the terminations is performed via internal DIP switches (see Fig. 2.4).
= 0   Not all Control Bus Terminations are ON;
= 1   All Control Bus Terminations are ON.

TERM OFF: Termination OFF bit. It refers to the termination of the CONTROL bus lines. The insertion or removal of the terminations is performed via internal DIP switches (see Fig. 2.4).
= 0   Not all Control Bus Terminations are OFF;
= 1   All Control Bus Terminations are OFF.

BERR FLAG (**V830**): Bus Error Flag Bit (meaningful in BLT/CBLT modes only). Reset after the readout of the Status Register .
= 0   board has not generated a Bus Error;
= 1   board has generated a Bus Error.

(Bits 8 to 15 are meaningless)

This Register can be accessed in D16 mode.

N.B.: the condition in which both TERM ON and TERM OFF bits are equal to 0 indicates an uncommon termination status, e.g. some terminations are ON and some are OFF.
In a daisy-chain controlled via the front panel CONTROL connector, one of the modules must have these terminations ON while all the others must have them OFF.

3.12. GEO Address Register

(Base Address + 0x1110, D16, read only; write cycles allowed for version without PAUX connector)

V820/V830 AA (PAUX): This register contains the geographical address of the module, i.e. the slot number picked up from the JAUX connector on the VME backplane. The register content is the following:
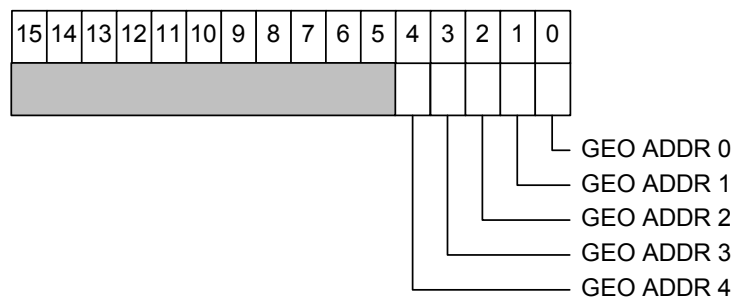

Fig. 3.11: Geographical address register

(Bits 5 to 15 are meaningless)

GEO [4...0] corresponds to A23...A19 address lines, with AM set to 0x2F: each slot has a relevant number whose binary encoding consists of the GEO ADDR 4 to 0. If a write access to the GEO register is performed in the versions with the PAUX connector, the module does not respond and the bus will go in timeout.

V820/V830 AC (NO PAUX): In the versions without the PAUX connector this register can be also written. In this case, the bits of the GEO Address register are set to 1 by default. In CBLT operation it is up to the User to write the correct GEO address of the module in this register before operating so that the GEO address will be contained in the HEADER words for data identification.

This Register supports D16 mode accesses only.

N.B.: In the case of versions without the PAUX connector, addressing via geographical address is not available.
Although in these versions it is possible to perform a write access to the GEO Address Register for data identification during CBLT operation (see § 4.6.6), avoid to use the GEO Address Register for addressing purposes.

N.B.: a write access to the GEO Address register causes a CLEAR of the module.

3.13. Interrupt Level Register
(Base Address + 0x1112, D16, read/write)

The 3 LSB of this register contain the value of the interrupt level (Bits 3 to 15 are meaningless). Default setting is 0x0. In this case interrupt generation is disabled.

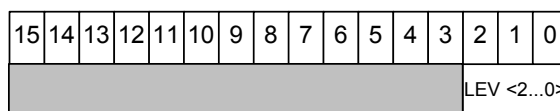| 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
													LEV <2...0>		

Fig. 3.12: Interrupt Level Register

This Register must be accessed in D16 mode. MCST access is also allowed.

3.14. Interrupt Vector Register
(Base Address + 0x1114, D16, read/write)

This register contains the STATUS/ID that the module INTERRUPTER places on the VME data bus during the Interrupt Acknowledge cycle (Bits 8 to 15 are meaningless). Default setting is 0xDD.
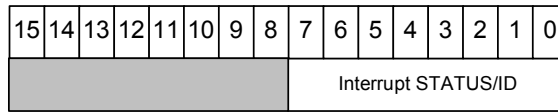
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								Interrupt STATUS/ID								

Fig. 3.13: Interrupt Vector Register

This Register must be accessed in D16 mode. MCST access is also allowed.

3.15. Address Decoder High Register (ADER High)
(Base Address + 0x1116, D16, read/write)

This register contains the A31...A24 bits of the address of the module: it can be set via VME for a relocation of the Base Address of the module. The register content is the following:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								A [31:24]								

Fig. 3.14: ADER HIGH Register

The Base Address relocation is activated by setting to 1 the ENABLE ADER register (see § 3.17). This Register must be accessed in D16 mode.

3.16. Address Decoder Low Register (ADER Low)
(Base Address + 0x1118, D16, read/write)

This register contains the A23...A16 bits of the address of the module: it can be set via VME for a relocation of the Base Address of the module. The register content is the following:
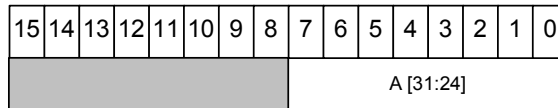
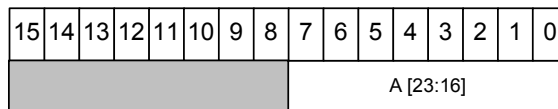| 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								A [23:16]								

Fig. 3.15: ADER LOW Register

The Base Address relocation is activated by setting to 1 the ENABLE ADER registers (see § 3.17). This Register must be accessed in D16 mode.

3.17. ENABLE ADER Register
(Base Address + 0x111A, D16, read/write)

This Register allows to activate the Base Address relocation. The GEO address is not influenced by the relocation.

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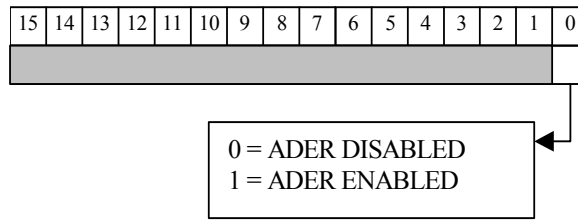| Document type:	Title:	Revision date:	Revision:
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Fig. 3.16: ENABLE ADER Register

ENABLE ADDRESS: Select Address bit.
= 0   base address is selected via Rotary Switch (default);
= 1   base address is selected via High and Low ADER registers.
This Register must be accessed in D16 mode.

N.B.: this register determines the base address variation of the module. Any VME accesses to the previous board's base address does not work.

3.18. MCST/CBLT Address Register

(Base Address + 0x111C, D16, read/write)

This register contains the most significant bits of the MCST/CBLT address of the module set via VME, i.e. the address used in MCST/CBLT operations.
The register content is the following:
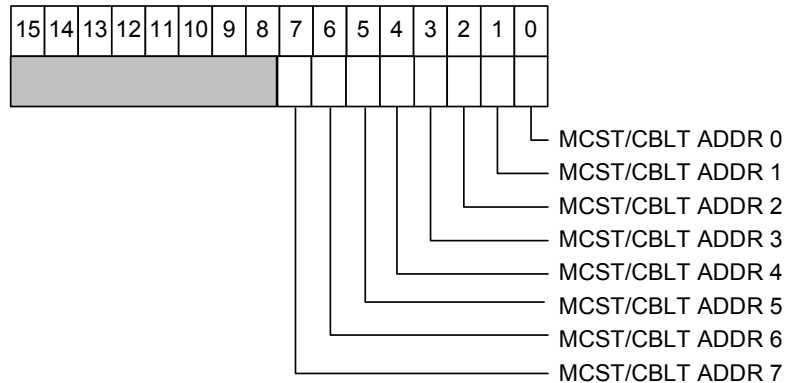

Fig. 3.17: MCST/CBLT address register

Default setting (i.e. at power ON or after hardware reset) is 0xAA: this address should not be set on other boards in the crate.

This Register must be accessed in D16 mode.

N.B.: a write access to this register causes the Counters Registers, the Trigger Counter and, for the Mod. V830, also the MEB and the MEB Event Number Register to be cleared.

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3.19. MCST/CBLT Control Register

(Base Address + 0x111E, D16, read/write)

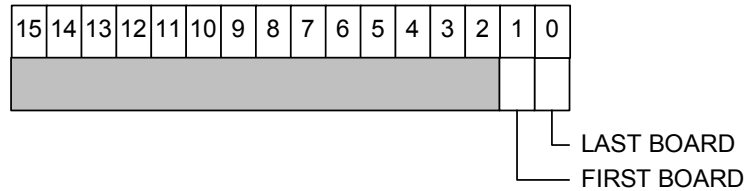This register allows performing some general MCST/CBLT settings of the module.

Fig. 3.18: MCST Control Register

LAST_BOARD   Last Board flag bit (valid in CBLT and MCST modes only)

FIRST_BOARD   First Board flag bit (valid in CBLT and MCST modes only)

The status of the boards according to the bit value is the following:

BOARD STATUS	FIRST BOARD bit	LAST BOARD bit
Board disabled in CBLT or MCST chain	0	0
First board in CBLT or MCST chain	1	0
Last board in CBLT or MCST chain	0	1
Active intermediate board in CBLT or MCST chain	1	1

(Bits 2 to 15 are meaningless).

N.B.: a write access to this register causes the Counters Registers, the Trigger Counter and, for the Mod. V830, also the MEB and the MEB Event Number Register to be cleared.

3.20. Software Reset Register

(Base Address + 0x1120, MCST, D16, write only)

A write access to this register allows performing a reset of the module (reset of counters, temporary buffers, MEB, Registers, etc.), **except** the following registers:

- ADER High;
- ADER Low;
- ENABLE ADER;
- MCST/CBLT Address
- GEO Address
- Dummy 16/32

This Register must be accessed in D16 mode. MCST access is also allowed.
This register allows to *restore* the module's default settings.

3.21. Software Clear Register

(Base Address + 0x1122, MCST, D16, write only)

A write access to this register allows performing a reset of the Counters Registers, the MEB, the Trigger Counter Register and the MEB Event Number Register.
This Register must be accessed in D16 mode. MCST access is also allowed.

3.22. Software Trigger Register

(Base Address + 0x1124, MCST, D16, write only)

When the module works with TRIGGER RANDOM enabled (bit 0 and 1 of the Control Register set respectively to 1 and 0, see § 3.8), a write access to this register allows to generate an internal trigger perfectly equivalent to an external one.
This Register must be accessed in D16 mode. MCST access is also allowed.

3.23. Trigger Counter (V830 only)

(Base Address + 0x1128, D32, read only)

This Register contains the number of occurred triggers starting from the last module clear in a 32-bit word, its 16 LSB are reported in the Header (if enabled).
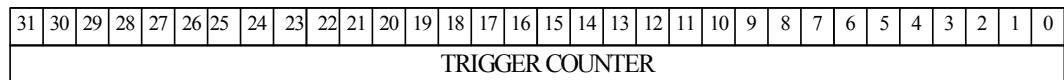
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															TRIGGER COUNTER																

Fig. 3.19: Trigger Counter Register

This Register must be accessed in D32 mode.

3.24. Almost Full Level Register (V830 only)

(Base Address + 0x112C, MCST, D16, read/write)

This Register allows the User to set the Almost Full Level of the MEB. When the MEB contains a number of words at least equal to the Almost Full Level, then an Interrupt Request (IRQ) is generated (if enabled) and the corresponding bit in the Status Register is set.

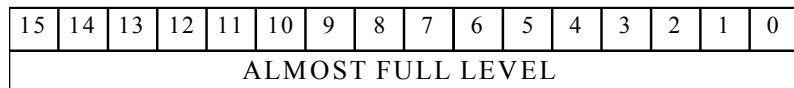| 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							ALMOST FULL LEVEL								

Fig. 3.20: Almost Full Level Register

The default Almost Full Level is 64 words. This Register can be accessed in D16 mode. MCST access is also allowed.

N.B.: A write access to this register causes the Counters Registers, the MEB, the Trigger Counter and the MEB Event Number Register to be cleared.

3.25. Firmware Revision Register

(Base Address + 0x1132, read only)

This register contains the firmware revision number coded on 8 bit. For example the REV. 3.2 would feature:

7	6	5	4	3	2	1	0
0	0	1	1	0	0	1	0
3				2			

FIRMWARE REVISION REGISTER

Fig. 3.21 Firmware Revision Register

3.26. MEB Event Number Register (V830 only)

(Base Address + 0x1134, D16, read only)

This Register contains the total number of events (Header must be enabled) stored in the MEB.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MEB Event Number															

Fig. 3.22: MEB Event Number Register

N.B.: The contents of this Register are meaningful only if the module is not in a BUSY state.

3.27. BLT Event Number Register

(Base Address + 0x1130, MCST, D16, read/write)

This register contains the number **Ne** of complete events which is desirable to transfer via BLT. The number of events must be written in a 8 bit word. The Register's default setting is 0, which means that the Event Aligned BLT is disabled (see § 4.6.4 and § 4.6.5). This Register must be accessed in D16 mode. MCST access is also allowed.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								BLT Event Number							

Fig. 3.23: BLT Event Number Register

N.B.: A write access to this register causes the Counters Registers, the MEB, the Trigger Counter and the MEB Event Number Register to be cleared.

3.28. Dummy32 Register

(Base Address + 0x1200, D32, read/write)

This register allows to perform 32 bit test accesses.

3.29. Dummy16 Register

(Base Address + 0x1204, D16, read/write)

This register allows to perform 16 bit test accesses.

3.30. ROM memory

(Base Address + 0x4000, D16, read only)

It contains some module's information according to the table below, such as:

- **OUI**:   manufacturer identifier (IEEE OUI)

- **Version**:   purchased version

- **Board ID**: Board identifier

- **Revision**: hardware revision identifier

- **Serial MSB**:   serial number (MSB)

- **Serial LSB**:   serial number (LSB)

Table 3.2: ROM Address Map for the Model V820/V830

Description	Address	Content (*)
OUI MSB	0x8026	**0x00**
OUI	0x802A	**0x40**
OUI LSB	0x802E	**0xE6**
Version	0x8032	**0x11**
BOARD ID MSB	0x8036	**0x00**
BOARD ID	0x803A	**0x03**
BOARD ID LSB	0x803E	**0x34**
Revision	0x804E	**0x00**
Serial MSB	0x8F02	**0x00**
Serial LSB	0x8F06	**0x02**

(*) the example of content for the relevant register refers to the Mod.V820 (serial number: 2; hardware revision: 0).

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4. Principles of operation

The models **V820** and **V830** are 32 channels Latching and Multievent Latching Scaler modules respectively.The TRIGGER signal latches "on the fly" the scalers data in a temporary buffer memory, readable via VME, without interfering on data acquisition process.
The model **V830** is equipped with a 32 kwords multievent buffer (MEB) memory which may be used to store the **EVENTS**: one EVENT, written in the memory after a TRIGGER, consists of an optional Header (see Fig. 3.19) and the block of data words (i.e. the counters' values at the TRIGGER time) coming from the selected channels (see § 3.6 for more details). The data transfer from the temporary buffer to the MEB memory requires a time of 1 μs. During this time the module is BUSY and it's not possible to accept any other incoming triggers. However, the input pulse counting continues without any bothering.

It's also possible to disable the TRIGGER via software and, in this case, the counters readout can be still performed "on the fly" via VME without interfering the data acquisition.

4.1. Extra control inputs

The module features some additional control input signals (see also § 2.4):
The **VETO** signal inhibits the counting of all the channels. It could be used for a hardware definition of "acquisition windows".
The **CLEAR** signal resets all the scalers (and the V830 MEB if the bit 6 of the Control Register is set) while the **TEST** signal allows to send a signal to all the channels.
A CLEAR can be also performed via a VME request.
Please note that the VETO signal does not inhibit the TEST pulse.
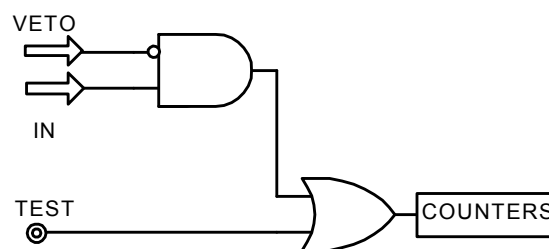The following diagram decribes the operation of the VETO and TEST pulses:

Fig. 4.1 Control inputs logic

N.B: If one channel logic status is "1", an eventual TEST pulse is neglected by the counters (see Fig. 4.1). Moreover, in the V820 / V830 LA / LC (<u>LVDS</u> inputs), if no input signal is present (i.e. the channels are disconnected), the TEST pulses are counted only if VETO is active, since in this case (<u>no signal</u>) the LVDS logic status is "1".

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4.2. Acquisition mode description

The modules V820 and V830 can operate in different acquisition modes:

- TRIGGER disabled   (**ACQ_MODE = 0**)
- TRIGGER random   (**ACQ_MODE = 1**)
- Periodical TRIGGER   (**ACQ_MODE = 2**)

The operating mode can be selected by setting bit 0 (ACQMODE Low) and bit 1 (ACQMODE High) of the Control Register (see § 3.8) as follows:

Table 4.1: Acquisition Mode selection

ACQ_MODE	ACQMODE L	ACQMODE H
0	0	0
1	0	1
2	1	0

4.2.1. TRIGGER disabled

After a channel reset by means of a CLEAR signal (external signal or VME request), the Control Register (see § 3.8) must be programmed such that **ACQ MODE = 0**.

The counters value can be read "on the fly" on VME request in D32 mode without interfering on the input pulses counting. Only one counter at once can be read out in this mode. The TRIGGER signals (internal or external) are disabled.
For Mod. **V830**, no data are written in the MEB and the module is never in a BUSY condition. BLT32, MBLT64, CBLT32/CBLT64 and Interrupt Request are not possible.
The channels' enabling is completely useless in this acquisition mode.

4.2.2. TRIGGER random

The Control Register (see § 3.8) must be programmed such that **ACQ MODE = 1**.

In this acquisition mode, a TRIGGER signal (external or from VME request) causes the "on the fly" latching of all the counters and the data writing in the temporary buffer. For Mod. **V820**, the data are available for the D32 VME readout at the counters' adress; data are loaded into the local buffer: this operation requires 150 ns and the module is BUSY during this time. Instead, for Mod. **V830**, the data accumulated in the enabled channels' counters are written in the local buffer and then transferred into the MEB memory. This operation requires 1 µs and the module is BUSY during this time. The data can be read from the MEB in D32, BLT32, MBLT64 or CBLT32/CBLT64.

During all the data writing phases, input pulses' counting proceeds although trigger signals would be neglected.

The Mod. **V830** will leave the BUSY status, on condition that the MEB is not full, only when the EVENT has been stored in the MEB (1 μs). Then the module is ready to accept a new incoming TRIGGER.

The Mod. **V820** has no MEB, so when a TRIGGER signal is performed, data are transferred from the counters into the temporary buffer, overwriting its content (i.e. the data transferred after the previous TRIGGER). Particular care is required in order to perform a VME readout *before a new TRIGGER occurs*.

4.2.3. Periodical TRIGGER (V830 only)

An internal programmable timer can send a periodical trigger signal. This mode is selected setting ACQ_MODE=2 in the Control Register (see § 3.8 for details). The trigger's period (dwell time) can be programmed in steps of 400 ns (see § 3.7 for programming details). Data are latched on the fly and then transferred from the temporary buffer to the MEB memory, every time a TRIGGER occurs. This operation requires 1 μs (so the dwell time should be programmed to be larger than this value) and the module is BUSY during this time. The data can be read from the MEB in D32, BLT32, MBLT64 or CBLT32/CBLT64.

4.3. Addressing capability

The modules can be addressed in three different ways, specifically:

1. via Base Address;
2. via GEOgraphical address;
3. via Multicast/Chained Block Transfer addressing mode.

4.3.1. Addressing via Base Address

The module works in A24/A32 mode. This implies that the module's address must be specified in a word of 24 or 32 bit. The Address Modifier codes recognised by the module are summarised in Table 4.2.

Table 4.2: Module recognised Address Modifier

A.M.	Description
0x3F	A24 supervisory block transfer (BLT)
0x3D	A24 supervisory data access
0x3C	A24 supervisory 64 bit block transfer (MBLT)
0x3B	A24 non privileged block transfer (BLT)
0x39	A24 non privileged User data access
0x38	A24 non privileged 64 bit block transfer (MBLT)
0x0F	A32 supervisory block transfer (BLT)
0x0D	A32 supervisory data access
0x0C	A32 supervisory 64 bit block transfer (MBLT)
0x0B	A32 non privileged block transfer (BLT)
0x09	A32 non privileged data access
0x08	A32 non privileged 64 bit block transfer (MBLT)

The Base Address can be selected in the range:

0x000000	←→	0xFF0000	A24 mode
0x00000000	←→	0xFFFF0000	A32 mode

The Base Address of the module can be fixed in two ways:

- by four rotary switches;
- by writing the Base Address in the ADER_HIGH and ADER_LOW registers.

The 4 rotary switches for Base Address selection are housed on two piggy-back boards plugged into the main printed circuit board (see Fig. 2.4).
To use this addressing mode the Enable Ader Register (see §3.17) must be set to 0. This is also the default setting.

The module Base Address can be also fixed by using the Ader_High and Ader_Low Registers. These two registers set respectively the A[31:24] and the A[23:16] VME address bits (see § 3.15 and 3.16).
To use this addressing mode the Enable Ader Register (see §3.17) must be set to 1.

4.3.2. *Geographical addressing for Mod. V820 AA / V830 AA (PAUX)*

The module works in A24 mode only. The Address Modifiers codes recognised by the module are:

AM=0x2F: A24 GEO access

All registers except for the MEB (i.e. the CR/CSR area) can be accessed via geographical addressing.
The geographical address is automatically picked up from the SN5..SN1 lines of the PAUX connector. Each slot of the VME crate is identified by the status of the SN5...SN1 lines: for example, the slot #5 will have these lines respectively at 00101 and consequently the module inserted in the slot #5 will have a GEO address set to 00101 (see Fig. 4.2).
The complete address in A24 mode for geographical addressing is:

A[31:24]	**don't care**
A[23:19]	**GEO**
A[18:16]	**0**
A[15:0]	**offset**

The following two figures show the binary and the hexadecimal representation of, respectively, the board Address and a Register Address (Bit Set Register) in GEO addressing mode.

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Binary representation
2				8				0				0				0				0				Hexadecimal representation

Fig. 4.2: Binary-Hexadecimal representation of the board Address in GEO mode (offset=0)

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	0	Binary representation
2				8				1006(offset)																Hexadecimal representation

Fig. 4.3: Binary-Hexadecimal representation of Bit Set Register Address in GEO mode

N.B.: In the case of versions where the SN5…SN1 lines are not available (i.e. the versions without the PAUX connector, named V820 AC and V830 AC), addressing via geographical address is not possible.
Although in these versions it is possible to perform a write access to the GEO Address Register (see § 3.12) for data identification during CBLT operation (see § 4.3.4), it is incorrect to use the GEO Address Register for addressing purposes when there is no PAUX.

4.3.3. Base/GEO addressing examples

The following is an example of Base/GEO Addressing for two V830 boards inserted in a VME crate.
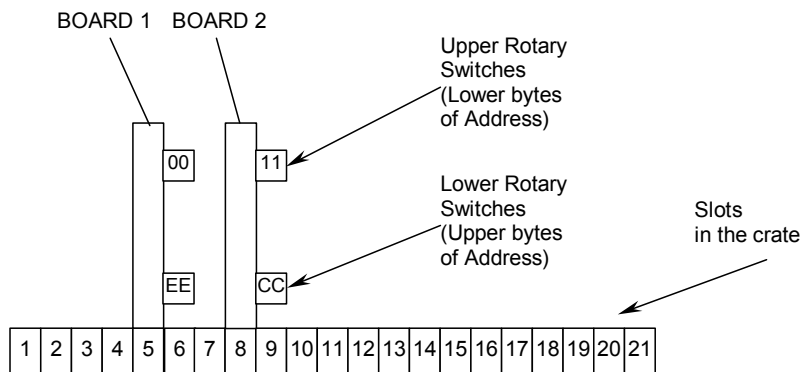

Fig. 4.4: Base/GEO Addressing: Example 1

If the board 1 and board 2 are respectively inserted in the slots 5 and 8 with the rotary switches for VME Base Addressing set as shown in the figure, the complete address of the registers of the two boards will be as follows:

Board 1:
Base addressing A32:   0xEE000000 + offset
Base addressing A24:   0x000000 + offset
GEO addressing A24:   0x280000 + offset (MEB excluded).

Board 2:
Base addressing A32:   0xCC110000 + offset
Base addressing A24:   0x110000 + offset
GEO addressing A24:   0x400000 + offset (MEB excluded).

4.3.4. MCST/CBLT addressing (CBLT for Mod. V830 only)

When the Multicast/Chained Block Transfer addressing mode is adopted, the module works in A32 mode only. The Address Modifiers codes recognised by the module are:

AM=0x0F: A32 supervisory block transfer (CBLT)
AM=0x0D: A32 supervisory data access (MCST)
AM=0x0B: A32 User block transfer (CBLT)
AM=0x09:   A32 User data access (MCST)

The boards can be accessed in Multicast Commands mode (MCST mode, see § 3.19), that allows to write in the registers of several boards at the same time by accessing the MCST Base Address in A32 only once.
The boards can be accessed in Chained Block Transfer mode (CBLT mode, see § 3.18) that allows to readout sequentially a certain number of contiguous boards in a VME crate. This access is allowed in BLT32 and BLT64 modes only to the MCST Base Address.

N.B.: The Base Address used for MCST and CBLT operations is the same, i.e. throughout this User's Manual the "MCST Base Address" identifies the same Address, used both for MCST commands (in Write only) and the CBLT Readout (in Read only, for the MEB, see § 3.2).

The MCST Base Address must be set in a different way from the ordinary Base Address. Its most significant byte (i.e. bits 31 through 24) must be written in the MCST/CBLT Address Register (see § 3.18) and must be set in common to all boards belonging to the MCST/CBLT chain. The default setting is 0xAA.

In MCST/CBLT operations, the IACKIN/ IACKOUT daisy chain is used to pass a token from one board to the following one. The board which has received the token stores/sends the data from/to the master via CBLT/ MCST access. No empty slots must thus be left between the boards or, in alternative, empty slots can be left only if VME crates with automatic IACKIN/IACKOUT short-circuiting are employed.
Once the addresses have been set, the first and last board in a chain must have, respectively, only the FIRST_BOARD (F_B) and only the LAST_BOARD (L_B) bit set to 1 in the MCST Control Register (see § 3.19). On the contrary, all intermediate boards must have both the FIRST_BOARD and the LAST_BOARD bits set to 1 (active, intermediate) or both the FIRST_BOARD and the LAST_BOARD bits set to 0 (inactive). By default these bits are set to 0 (the board is inactive).

Board status	Board position in the chain	F_B bit	L_B bit
inactive	-	0	0
active	last	0	1
active	first	1	0
active	intermediate	1	1

Please note that in a chain there must be one (and only one) *first board* and one (and only one) *last board*.

The complete address in A32 mode is:

A [31:24]   MCST/CBLT Address
A [23:16]   0
A [15:0]   offset

N.B.: In CBLT operation the data coming from different boards are tagged with the HEADER containing the GEO address in the 5 MSB (see § 3.2). In the versions without the PAUX connector it is up to the User to write the GEO address in the GEO register (this operation is allowed <u>only if</u> the PAUX is not present) before executing the CBLT operation. If the GEO address is not written in the relevant register before performing the CBLT operation, it will not be possible to identify the module which the data are coming from.

4.3.5. MCST/CBLT addressing examples

The following is an example of MCST and CBLT addressing for four V830 boards plugged into a VME crate. To access the boards the steps to be performed are as follows:

1. Set the MCST address (see § 3.18) for all boards via VME Base Address or geographical addressing (if available);

2. Set the bits F_B and L_B of the MCST Control Register (see § 3.19) according to the operational status (active or inactive) of each board and to its position in the chain (first, intermediate or last);

3. Write or read the boards via MCST/CBLT addressing.

An example of User procedures which can be used to perform a write access is:

vme_write (address, data, addr_mode, data_mode),

which contain the following parameters:

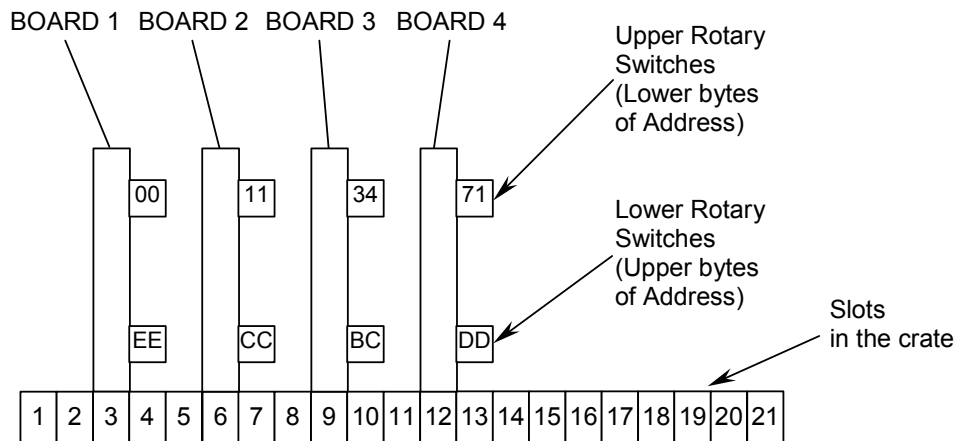|	
Address:	the complete address, i.e. Base Address + offset;
Data:	the data to be either written or read;
Addr_mode:	the addressing mode (A32, A24 or GEO);
Data_mode:	the data mode (D16, D32 or D64).

Fig. 4.5: MCST/CBLT Addressing Example

In the following two software examples using the above mentioned procedures are listed (the module's reset for Boards 1, 2 and 4 is performed via MCST):

Example of Access via Base Address

```
vme_write (0xEE00111C, 0xAA, A32, D16)   /* set MCST Address=0xAA for board 1 */
vme_write (0xCC11111C, 0xAA, A32, D16)   /* set MCST Address=0xAA for board 2 */
vme_write (0xBC34111C, 0xAA, A32, D16)   /* set MCST Address=0xAA for board 3 */
vme_write (0xDD71111C, 0xAA, A32, D16)   /* set MCST Address=0xAA for board 4 */
vme_write (0xEE00111E, 0x02, A32, D16)   /* set  board 1 = First */
vme_write (0xCC11111E, 0x03, A32, D16)   /* set  board 2 = Active */
vme_write (0xBC34111E, 0x00, A32, D16)   /* set  board 3 = Inactive */
vme_write (0xDD71111E, 0x01, A32, D16)   /* set  board 4 = Last */
vme_write (0xAA001120, 0x80, A32, D16)   /* perform a RESET on all the boards */
```

Example of Access via geographical address

```
vme_write (0x18111C, 0xAA, GEO, D16)   /* set MCST Address=0xAA for board 1 */
vme_write (0x30111C, 0xAA, GEO, D16)   /* set MCST Address=0xAA for board 2 */
vme_write (0x48111C, 0xAA, GEO, D16)   /* set MCST Address=0xAA for board 3 */
vme_write (0x51111C, 0xAA, GEO, D16)   /* set MCST Address=0xAA for board 4 */
vme_write (0x18111E, 0x02, GEO, D16)   /* set board 1 = First */
vme_write (0x30111E, 0x03, GEO, D16)   /* set board 2 = Active */
vme_write (0x48111E, 0x00, GEO, D16)   /* set board 3 = Inactive */
vme_write (0x51111E, 0x01, GEO, D16)   /* set board 4 = Last */
vme_write (0xAA001120, 0x80, A32, D16)   /* perform a RESET on all the boards */
```

N.B.: there must be always one (and only one) FIRST BOARD and one (and only one) LAST BOARD.

4.4. Interrupter capability (Mod. V830 only)

The Mod. V830 (provided with the MEB) houses a VME INTERRUPTER. The INTERRUPTER responds to 8 bit, 16 bit and 32 bit Interrupt Acknowledge cycles producing an 8-bit STATUS/ID on the VME data lines D00..D07.

4.4.1. Interrupt Status/ID

The interrupt STATUS/ID is 8-bit wide, and it is contained in the 8LSB of the Interrupt Vector Register (see § 3.14). The register is available at the VME address: Base Address + 0x1114.

4.4.2. Interrupt Level

The interrupt level corresponds to the value stored in the 3LSB of the Interrupt Level Register (see § 3.13). The register is available at the VME address: Base Address + 0x1112. If the 3LSB of this register are set to 0, the Interrupt generation is disabled.

4.4.3. Interrupt Generation

An Interrupt request is generated whenever the condition ALMOST FULL (marked with a bit) of the MEB is reached (see § 3.24 and § 3.26). ALMOST FULL level is set by the user (default: 64 words).

4.4.4. Interrupt Request Release

The INTERRUPTER removes its Interrupt request either when a read access is performed to the MEB so that the number of events stored in the memory decreases and becomes lower than the value written in the Almost Full Level Register or when a module's *clear* is performed (see § 3.8, § 3.9, § 3.10, § 3.20 and § 3.21).

4.5. Data transfer capability

The internal registers can be accessed in D16/D32 mode, according to which is specified in § 3.1. Accesses in D32, BLT32, MBLT64, CBLT32 and CBLT64 are available for the MEB (V 830 only).

4.6. Readout modes (Mod. V830 only)

The Mod. V830 MEB can be readout via VME in D32, BLT32, BLT64, CBLT32 and CBLT64. The module has to be programmed in order to work in the required mode, and some parameters have to be set in order to keep data aligned (i.e. to transfer an integer number of events per cycle). In the following each readout mode will be described in detail.

Nw is the number of word which compose an event and **Nch** is the number of the enabled channels; if the header is enabled Nw=Nch+1, otherwise Nw=Nch (see § 3.6 and § 3.8). When the module is switched on or when a hardware/software reset is performed, the MEB is empty and if read out it would return a non significant. **It's up to the user to verify the presence of valid data in the MEB before read out**; this can be performed via the Status Register read out (*Data Ready Bit*, see § 3.11). When a trigger signal occurs, an event, composed of a header (optional) and a number of data equal to the number of enabled channels, is loaded into the MEB (see also § 3.6 and § 3.8).

4.6.1. D32 MEB readout

- *Berr Disabled*: If the MEB is read out when empty, a non-valid data is returned.
- *Berr Enabled*: If the MEB is read out when empty, BERR is signalled.

4.6.2. BLT32/64 MEB readout with Bus Error and Event Aligned BLT disabled

BLT32/64 readout with BERR and Event Aligned BLT mode disabled does not permit to collect one or more complete events since the number of bytes **Nb** which are transferred in a BLT cycle has usually a "typical" value (256, 2048…) which rarely coincide with a multiple of the number of bytes **NB** composing an event, i.e. NB=Nw·4 (see § 4.6). It is more than likely that in a BLT cycle an event could be partially read out and the remaining part would be read out in the subsequent cycle. If the MEB contains a number N of words smaller than Nb/4 (the number of words readout in BLT cycle), the module transfers its memory content, completed with (Nb/4)-N non-valid data. If the Header is enabled the non-valid data are replaced by "fillers" (for Mod. V830, a filler's value is 0).
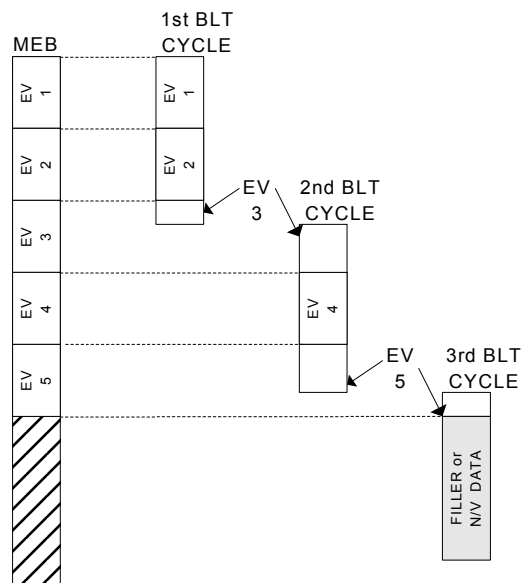

Fig. 4.6 Example of BLT data transfer with BERR and Event Aligned BLT disabled

4.6.3. BLT32/64 MEB readout with Bus Error enabled

In this mode the module produces a BERR signal (see § 3.8) once the last data in the MEB has been transferred and no filler is added.
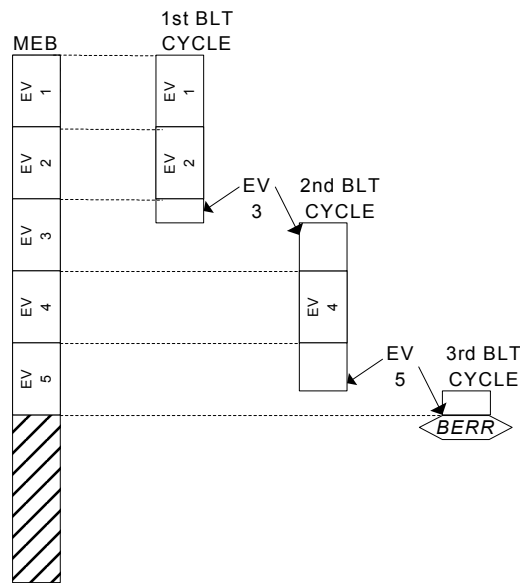
Fig. 4.7 Example of BLT data cycle with BERR enabled and Event Aligned BLT disabled

4.6.4. BLT32/64 MEB readout with Event Aligned BLT enabled

This mode allows to transfer an integer number **Ne** of events, set via the BLT Event Number Register (see § 3.27). **The Header must me enabled**. The default setting value of this register is 0, so this mode disabled. In order to enable the Event Aligned BLT the desired number of events Ne must be written in the BLT event number register then the header must be enabled. This mode allows the module to transfer a maximum number Ne of events; three cases may occur:

- The memory has a number of events smaller than Ne: the module transfers its memory content and completes the cycle adding fillers (filler =0).
- The memory has a number of events larger than Ne and Nb/4>Ne (where Nb/4 is the number of words transferred in one BLT cycle): the module transfers Ne events and completes the cycle adding fillers.
- The memory has a number of events larger than Ne and Nb/4<Ne: the transfer requires more than one cycle to be completed, the last cycle is completed with fillers.

Anytime a value is written in the BLT Event Number Register a module's *clear* is performed.
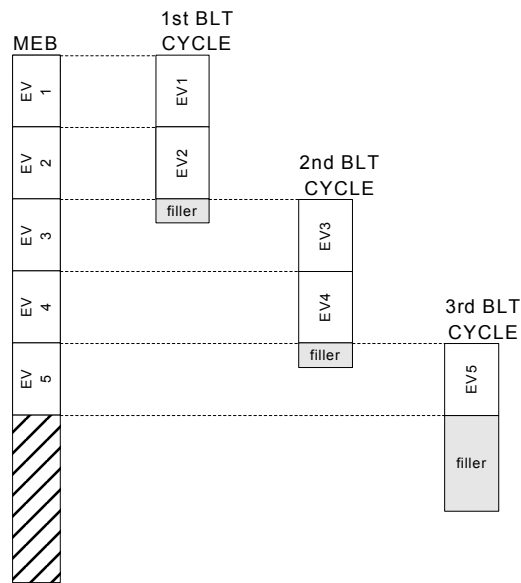
Fig. 4.8 Example of BLT data cycle with BERR disabled and Event Aligned BLT enabled

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4.6.5. BLT32/64 MEB readout with both Event Aligned BLT and Bus Error enabled

This mode allows the module to transfer a maximum number Ne of events; **the Header must be enabled**, three cases may occur:

- The memory has a number of events smaller than Ne: the module transfers its memory content then asserts BERR, thus terminating the cycle.

- The memory has a number of events larger than Ne and Nb/4>Ne: the module transfers Ne events then asserts BERR thus terminating the cycle.

- The memory has a number of events larger than Ne and Nb/4<Ne: the transfer requires more than one cycle to be completed.

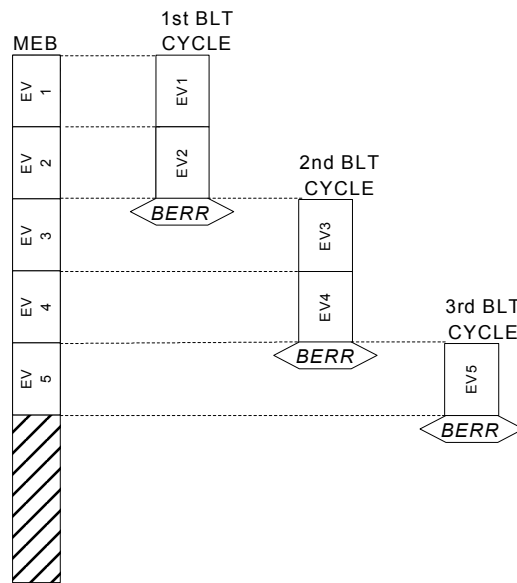**N.B.: Enabling the BERR is useful in order to save time, avoiding fillers' transfer.**

Fig. 4.9 Example of BLT data transfer with BERR and Event Aligned BLT enabled

4.6.6. *CBLT32/64 MEB readout*

The CBLT mode allows data readout from a set of modules in the crate. The header must be enabled in order to perform the cycle. The readout starts from the first module of the set: it transfers its first event, then passes the *token* to the subsequent module via the IACKIN/IACKOUT daisy chain lines. If one module's MEB is empty or *Inactive* (see § 3.19), the token is passed with no data transfer. If the data transfer is not completed by the first CBLT cycle, a second one may be attached to the first and so on until the last module in the set has transferred its last data: then it asserts BERR, which is automatically enabled when the CBLT is performed, thus completing the cycle.

CBLT64: if an odd number of words is transferred, the CPU completes the cycle adding a word composed of fillers.